Amendments to the Specification

Please amend the specification as follows:

[0006] Please delete.

[0023] Using the technique 100, or similar techniques, a user can specify a particular number of data fields for collection analysis. The user can also synchronize the timing of the collection process. In the technique 100, if a sufficient number of data fields has not been collected, the software routine 100 can again enable the CRC to receive ~~and accumulate~~ an additional data field as illustrated in block 110. Once the desired field count has been reached, all of the accumulated CRCs are examined, as illustrated in block 112.

[0028] As shown in FIG. 2, data field segments 202 and 204 are separated by a synchronization marker 210. The segments 204 and 206 are separated by a synchronization marker 212. And the segments 206 and 208 are separated by a synchronization marker 214. During bench testing, however, CRC module enablement can occur for example at a time 216, as indicated in FIG. 2. ~~CRC enablement at the time 216 occurs because the bench testing method does not always know when the synchronization markers occur.~~

[0030] FIG. 3 provides a block diagram illustration 300 of an exemplary CRC checksum system 300 constructed and arranged in accordance with an embodiment of the present invention. In particular, the CRC checksum system 300 enables bench testers to selectively program a <u>desired</u> ~~desirable~~ field count and provide synchronism between CRC module enablement and an occurrence of synchronization markers. This particular technique eliminates the problems noted above with regard to conventional bench testing.

[0031] In FIG. 3, an external memory device 302, such as a register, is added to a conventional video bench test set up. The register 302 is configured to receive as an input a desired numeric field count value 304. The field count value 304 enables a user to specifically program the number of field counts desired to perform CRC check sum analysis. During CRC check sum analysis, the desired ~~desirable~~ field count value 304 is loaded into a comparator 306 for comparison with an actual field count value.

[0035] Next, the detector 312 senses a presence of the synchronization marker 210, and nearly simultaneously, provides a CRC module interrupt 400 ~~402~~ to enable the CRC module 308. The synchronization marker 210 indicates a beginning of the first collected data segment 204. After the two segments 204 and 206 have been received by the CRC module 308, the CRC module disablement command 320 is sent to the detector 312. The detector 312 then senses the synchronization marker 214, indicating an end of the data field segment 214 and substantially simultaneously disables the CRC module 308. The CRC module 308, now having two complete data fields, 204 and 206 collected therein, will load their associated accumulated check sums into the register 324.

[0038] The present invention provides a function that enables a user to specify a programmable number of field counts for a CRC module to analyze ~~record~~ the CRC check sum. It contains one register that specifies a number of fields to be recorded and a bit to enable the CRC analysis. Once CRC analysis has been enabled, the associated hardware will start performing CRC analysis at the next pixel start and continue to record the check sum until the specified number of fields has been analyzed ~~recorded~~. It terminates check sum analysis at the end of that specified field count.